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10/754,483	01/09/2004	Kevin Conley	SDK1P017/503	6185

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BEYER LAW GROUP LLP/ SANDISK
P.O. BOX 1687
CUPERTINO, CA 95015-1687

EXAMINER	
CAMPOS, YAIMA	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/754,483	CONLEY ET AL.	
	Examiner	Art Unit	
	YAIMA CAMPOS	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10/2/08*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25 and 36-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25,36-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. As per the instant Application having Application number 10/754,483, the examiner acknowledges the applicant's submission of the amendment dated October 2, 2008. At this point, claims 1, 13 and 19 have been amended, claims 26-35 have been canceled, and claims 36-38 have been added. Claims 1-25 and 36-38 are pending.

Continued Examination Under 37 CFR 1.114

2. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on October 2, 2008 has been entered.

OBJECTIONS TO THE CLAIMS

3. **Claims 36-38** are objected to because of the following informalities:

4. Claims 36-37 recited the term "forth address region," which is believed to be a typographical error and should be corrected to read "fourth address region".

5. Appropriate correction is required.

REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. **Claims 1-10, 13-14, 17-25 and 36-38** are rejected under 35 U.S.C. 103(a) as being unpatentable over Suda (US 2004/0123059) in view of Moro (US 2004/0107316) and Murray et al. (US 6,185,666).

8. As per **claim 1**, Suda discloses "A method for reading data from a memory card that provides non-volatile data storage, defined by a contiguous range of addresses" as **["the present invention relates to a memory card authentication system, a memory card host device, a memory card, a storage area switching method, and a storage area switching program, which are capable of switching plural storage areas" (Page 1, paragraph 0003) address space within memory card 3 (See Figure 1) and (Figure 5)]**
"said method comprising: (a) accessing volume information stored in a range of addresses that is a part of the contiguous range of addresses that defines the address space, the contiguous range of the address space **being capable of** {*interpreted as intended use, see MPEP 2106 II-C*} storing either the volume information or user data depending on the configuration of the memory card; **["It is possible to allow the memory card host device 1 to execute a procedure for reading out internal register values of the memory card and a procedure for judging whether or not the memory card has plural storage areas by mean of reading out the storage switching program form the program storage device" (Page 2, Paragraph 0027) and "at least one internal register 12a with a flag indicating the quantity of the storage areas added to a reserved area thereof" (Page 2, Paragraph 0028)]**. Applicant should note that as the "internal register 18" stores the number of areas inside a memory card, this number of

areas corresponds to the claimed "volume information." The number of areas inside a memory card represents the number of volumes inside a memory card, and therefore, represents "volume information." Furthermore, Suda discloses **[*"FIG. 1 shows the conventional memory card, in which flags are added to convention reserved areas. Each of the internal registers 12a, 12b, 12c, and 12d of the memory card 3 includes first to third bit string 20a, 20b, and 20c... The first bit string 20a equivalent to the first 23 bits of the internal register indicates a characteristic of the memory card... The second bit string 20b equivalent to the first 23 bits of the internal register indicates a characteristic of the memory card 3… The third bit string 20c equivalent to 4 bits subsequent to the second bit string is also a convention reserved area of the internal register... Information indicating the quantity of storage areas is added hereto... In the memory card 3, shown in FIG. 1, a flag indicating 4 is et to each of the third bit strings of the internal register... when the memory card 3 has four storage areas*" (Par. 0039; See Figure 1 and related text)].** Applicant should note that Examiner interprets the "first storage areas 11a-12a, 11b-12b, 11c-12c and 11d-12d" as a continuous address space which is shown as bit strings comprising fields 20a, 20b and 20c. Therefore, as Suda stores volume information indicating the number of storage areas within field 20c of internal registers, which are shown to comprise contiguous range of addresses. Applicant should further note that Suda expressly discloses **[**"FIG. 5 shows the memory card 3 in which the plural storage areas 11a, 11b, and 11c severally include the internal registers 12a, 12b, and 12c" (Figure 5 and related text) wherein contiguous address space comprising addresses 00000-xFFFF is shown to include/encompass both storage areas 11a, 11b, 11c and internal registers 12a, 12b, and 12c, as shown in the citation above (Note that the drawing in Figure 5, included dashed**

lines does not exclude internal registers from address space shown on the left)]. Further, any memory/storage device is "capable of" storing any type of data. Furthermore, claims 1, 13 and 19 require that the contiguous range of the address space store either user data OR system configuration data, which is taught by Suda **[See above]**.

(b) determining, based on the volume information, whether the non-volatile data storage has a first configuration having a multiple volume address space corresponding to a first file format or a second configuration having a single file format volume address space corresponding to a second file format;" **[With respect to this limitation, Suda discloses that "the memory card host device 1 includes a plural area authentication module 21 for judging whether or not a memory card subject to exchanging information has plural storage areas therein" (Figure 1 and Page 2, paragraph 0027, lines 1-4) wherein "it is possible to maintain compatibility with a conventional memory card host device by setting the storage area having the file system that can be controlled by the conventional memory card host device as the storage area accessible when the power supply is turned on. Regarding the other storage areas, it is possible to moderate limitations of the storage capacities by changing the file systems thereof into file systems adopting new methods" (Page 5, paragraph 0066). Suda also explains that the size of storage areas "does not exceed the marginal capacity which can be handled by using a single file system. For example, when the FAT 16 is used as the file system, the marginal capacity is equal to 2 gigabytes" (Page 2, paragraph 0028, lines 14-17) and that "a conventional command length can only express an address up to the second storage area 11b. However, with the use of the address expressed with blocks enables expression of a large-capacity address" (Figure 5 and Page 4, paragraph 0057, lines 17-20);**

therefore, multiple volume address space has a first file format and single volume address space having a second file format]

(c) operating the memory card in accordance with the first file format by dividing the address space of the non-volatile data storage into a plurality of volumes when said determining (b) determines that the memory card has the first configuration, each of the plurality of volumes containing that volume information stored in a respective range of addresses therein; and **[Suda discloses this limitation as when judgment determines that a plurality of storage areas exist, then "the memory card switches storage areas so as to refer to a desired storage area" (Page 3, paragraph 0034, lines 1-3) and explains that "when the area has changed normally," then "data processing of the memory card by the memory card host device is performed" (Page 3, paragraph 0035, lines 8-10); thereby, operating the memory card as having a plurality of volumes wherein storage registers in each volume store volume information for each volume (See Above)]**

"(d) operating the memory card in accordance with the second file format by accessing when said determining (b) determines that the memory card has the second configuration **[With respect to this limitation, Suda discloses "where a judgment is made that there is only a single storage area, then normal processing takes place" (Pages 2-3, paragraph 0033, lines 10-11) and explains "in a memory card host device which cannot perform the above-described processing, the memory card remains in the state as shown in Fig. 4A when the power supply is turned on. Accordingly, such a memory card host device handles the memory card as the memory card having only the first storage area 11a" (Page 4, Par. 0050); thereby, operating the memory card as having a single volume]**

Assuming (*for the sake of argument*) that Suda's internal registers were not included in the address space defined by the contiguous range of addresses 00000 through xFFFF, as argued by Applicant, it would be obvious to one of ordinary skill in the art to place internal registers within this range or anywhere within memory card 3, since it involves a simple relocation of parts and it has been held that rearranging parts of an invention involves only routine skill in the art. *In re Japikse,* 86 USPQ 70.

Suda does not disclose expressly "(d) operating the memory card in accordance with the second file format **by accessing the entire address space** of the non-volatile data storage as the single volume when said determining" nor "each range of addresses which stores the volume information in a second and any subsequent volumes under the first configuration stores user data under the second configuration."

Moro discloses "(d) operating the memory card in accordance with the second file format by accessing the entire address space of the non-volatile data storage as the single volume when said determining (b) determines that the memory card has the second configuration, as **["the capacity switching-type memory card host device 12 performs a setting to make the first partition 162 and the second partition 163 accessible as a single partition… Concrete examples of the method for setting of the single partition are shown in FIG. 6... logically connecting three partitions of C: 801, D: 802, and E:803 and thereby qualifying these partitions collectively as a single partition C': 804" (par. 0038; figs. 1 and 6 and related text)]**.

Murray discloses operating a memory as multiple volumes or as a single volume wherein when changing from operating the memory as multiple volumes to operating the memory as a

single volume, "each range of addresses which stores the volume information in a second and any subsequent volumes under the first configuration stores user data under the second configuration" as **[merging two or more adjacent partitions to create a single or target partition wherein one or more FAT 16 partitions may be merged into a FAT 32 partition (col. 4, lines 37-55) and explains "a FAT files system normally places file system data 402 at or near the left edge of the partition; user data and available space (if any) take up the rest of the partition 400. The FAST file system data 402 in a target partition is modified when two or more FAT partitions are merged" (col. 7, lines 13-20) wherein "If the merged partition is to be a FAT partition, then the left-most partition is preferably considered the target partition because the merged FAT partition always places the combined system data on the left-hand side (near the start of the merged partition)" (col. 13, lines 18-46) "the target partition can be grown by moving its right edge (end)" (col. 10, lines 34-53). Also see (col. 15, line 57-col. 16, line 4; col. 17, line 63-col. 18, line 11; col. 18, lines 38-47). Murray also explain that data previously holding system data in a secondary partition is deleted to create free space for files/user data in the target partition (col. 20, line 23-col. 21, line 3). Also refer to (col. 22, line 45-col. 24, line 58)]**.

Suda, Moro and Murray are analogous art because they are from the same field of endeavor of memory access and control.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify the memory card which can be accessed in either multiple mode or single mode, as described by Suda, and more specifically combine the multiple memory areas as a single memory area when using the memory card as a single volume, as taught by Moro and

further "each range of addresses which stores the volume information in a second and any subsequent volumes under the first configuration stores user data under the second configuration."

The motivation for doing so would have been because Moro discloses providing the a memory card that can be used as multiple partitions or as a single partition provides the advantage of **[being able to increase the capacity of a memory and facilitate user access (pars. 0007 and 0038)]** and Murray discloses under a FAT files system, system information must be stored at the beginning of the volumes; thus, when combining two partitions into a target partition, system data must be moved to the beginning of the target partition and the rest is of the area is freed to store files/user data as needed **[(col. 13, lines 18-46; col. 4, lines 37-55; col. 7, lines 13-20; col. 10, lines 34-53; col. 15, line 57-col. 16, line 4; col. 17, line 63-col. 18, line 11; col. 18, lines 38-47; col. 22, line 45-col. 24, line 58)]**.

Therefore, it would have been obvious to combine Suda with Moro and Murray for the benefit of creating a method for reading data from a memory card to obtain the invention as specified in claim 1.

9. As per **claim 2 and 21**, the combination of Suda, Moro and Murray discloses "A method as recited in claims 1 and 20," **[See rejection to claim 1 above and rejection to claim 20 bellow]** "wherein the memory card includes a switch that has a plurality of switch positions," **[With respect to this limitation, Suda discloses "a large-capacity memory card which is arranged to switch plural storage areas with the use of mechanical switches provided on a housing" (Page 5, paragraph 0068 and paragraph 0069 (*see bellow*))]** "and wherein said operating (c) includes at least: (c1) determining a switch position for the switch; and (c2)

selectively enabling one of the plurality of volumes based on the switch position" **[Suda discloses this limitation as "It is possible to select any one of the storage areas 11a and 11b of the memory card 3 by use of the mechanical switches 16a and 16b provided on the housing of the memory card 3. For example, when the mechanical switches 16a and 16b are set to positions marked as "1", the controller 10 reflects the state of the switches to the first internal register 12a, thereby allowing a memory card host device to handle the first storage area 11a. Similarly, when the mechanical switches 16a and 16b are set to positions marked as "2", the controller 10 reflects the state of the switches to the internal register 12a, thereby allowing the memory card host device to handle the second storage area 11b. Although FIG. 7 schematically shows the single internal register 12a, it is acceptable if the memory card 3 includes the plural internal registers 12a, 12b, 12c, and 12d for the respective plural storage areas as shown in FIG. 1. Alternatively, it is also acceptable that the memory card 3 includes the internal register 18 for the plural storage areas as shown in FIG. 3" (Page 5, paragraph 0069)]**.

10. As per **claims 3 and 4**, the combination of Suda, Moro and Murray discloses "A method as recited in claim 2," **[See rejection to claim 2 above]** "wherein the switch has at least a first position and a second position, and wherein said operating (c) further includes at least:" **[See rejection to claim 2 above]** "(c3) imposing an address offset when the switch is in the second position; wherein the address offset enables the memory card to provide more data storage capacity than available with a file system using 16-bit addressing" **[Suda discloses this concept as "it is possible to maintain compatibility with a conventional memory card host device by setting the storage area having the file system that can be controlled by the conventional**

memory card host device as the storage area accessible when the power supply is turned on. Regarding the other storage areas, it is possible to moderate limitations of the storage capacities by changing the file systems thereof into file systems adopting new methods" (Page 5, paragraph 0066). Suda also explains that the size of storage areas "does not exceed the marginal capacity which can be handled by using a single file system. For example, when the FAT 16 is used as the file system, the marginal capacity is equal to 2 gigabytes" (Page 2, paragraph 0028, lines 14-17) and that "a conventional command length can only express an address up to the second storage area 11b. However, with the use of the address expressed with blocks enables expression of a large-capacity address" (Figure 5 and Page 4, paragraph 0057, lines 17-20)].

11. As per **claim 5**, the combination of Suda, Moro and Murray discloses "A method as recited in claim 2, wherein the switch has at least a first position and a second position," **[See rejection to claim 2 above]** "wherein, when the switch position is in the first position and the memory card is operated by dividing the address space of the non-volatile data storage into the plurality of volumes, the first volume of the non-volatile data storage is accessed, and wherein, when the switch position is in the second position and the memory card is operated by dividing the address space of the non-volatile data storage into the plurality of volumes, a second volume of the non-volatile data storage is accessed" **[With respect to this limitation, Suda discloses that "It is possible to select any one of the storage areas 11a and 11b of the memory card 3 by use of the mechanical switches 16a and 16b provided on the housing of the memory card 3. For example, when the mechanical switches 16a and 16b are set to positions marked as "1", the controller 10 reflects the state of the switches to the first internal register 12a,**

thereby allowing a memory card host device to handle the first storage area 11a" (Page 5, paragraph 0069) as changing the position of a switch to select different memory regions].

12. As per **claim 6**, the combination of Suda, Moro and Murray discloses "A method as recited in claim 5," **[See rejection to claim 5 above]** "wherein the memory card is formatted into either one of a single volume or a pair of volumes, the pair of volumes being the first volume and the second volume" **[With respect to this limitation, Suda discloses that "where a judgment is made that there is only a single storage area, then normal processing takes place" (Page 3, paragraph 0033, lines 10-11) as an instance when a memory card is manages as a single storage area. Suda also discloses that when judgment determines that a plurality of storage areas exist, then "the memory card switches storage areas so as to refer to a desired storage area" (Page 3, paragraph 0034, lines 1-3) and explains that "when the area has changed normally," then "data processing of the memory card by the memory card host device is performed" (Page 3, paragraph 0035, lines 8-10) as having a plurality of volumes]**. Moro discloses **[accessing memory card 32 as two partitions 162 and 163 or combining these two partitions and accessing partitions 162 and 163 as a single partition (figs. 1 and 6 and related text; par. 0038)]**.

13. As per **claims 7, 10, and 17**, the combination of Suda, Moro and Murray discloses "A method as recited in claims 6, 13 and 28," **[See rejection to claim 6 above and rejection to claims 13 and 28 below]** "wherein the total non-volatile data storage for the memory card is formatted into the first volume of X gigabytes as the single volume, or formatted into the first and second volumes of X/2 gigabytes each as the pair of volumes" **[Suda discloses this concept as a memory card that can have either a single storage area or a plurality of storage areas**

wherein "The size thereof does not exceed the marginal capacity which can be handled by a single file system. For example, when the FAT 16 is used as the file system, the marginal capacity is equal to 2 gigabytes. In this event, the marginal capacity of the entire memory card is equivalent to 8 gigabytes when the memory card includes four storage areas as shown in FIG. 1, and is 10 gigabytes when the memory card includes five storage areas or 12 gigabytes when the memory card includes six storage areas" (Page 2, paragraph 0028) as having different memory capacities, depending on the number of partitions/storage areas within a memory card]. Moro discloses **[accessing memory card 32 as two partitions 162 and 163 or combining these two partitions and accessing partitions 162 and 163 as a single partition (figs. 1 and 6 and related text; par. 00380)]**.

14. As per **claims 8 and 9**, the combination of Suda, Moro and Murray discloses "A method as recited in claim 1," **[See rejection to claim 1 above]** "wherein said method further comprises: (e) detecting activation of the memory card, and wherein said accessing (a), said determining (b), and said operating (c) or (d) are performed once said detecting (e) detects the activation of the memory card" wherein "the activation of the memory card occurs upon power-on of the memory card or upon insertion of the memory card into a host device" **[With respect to this limitation, Suda discloses "a memory card authentication system according to the first embodiment of the present invention includes a memory card host device 1, a memory card 3, and a bus 2 for transmitting and receiving data" (Page 2, paragraph 0026) and also discloses, "the memory card 3 as shown in fig. 4A is in a state where the power supply is turned on. In this event, it is possible to handle the first storage area 11a" (Page 4, paragraph 0049)]**. See Kim **[(Page 1, Par. 0006 and 0009 and Figure 1 and related text)]**.

15. As per **claims 13-14, and 24**, Suda discloses "A memory card having a single memory array defined by a contiguous range of addresses **capable of being configured** {*interpreted as intended use, See MPEP 2106 II-C*} as multiple partitions each having a first size or as a single partitions each having a second size, said memory card comprising:" as **["the present invention relates to a memory card authentication system, a memory card host device, a memory card, a storage area switching method, and a storage area switching program, which are capable of switching plural storage areas" (Page 1, paragraph 0003); and also teaches that "the memory card host device 1 includes a plural are authentication module 21 for judging whether or not a memory card subject to exchanging information has plural storage areas therein" (Figure 1 and Page 2, paragraph 0027, lines 1-4) and explains that "it is possible to handle a storage capacity larger than the marginal capacity of the file system by means of providing plural storage areas" (Page 2, paragraph 0030, lines 1-4) address space within memory card 3 (See Figure 1) and (Figure 5)]**

"non-volatile data storage that provides data storage having an address space, said address space being configured to include at least a first partition, the first partition including partition information that is stored in a range of addresses that is part of the contiguous range of addresses, the contiguous range of the addresses **being capable of** {*interpreted as intended use, See MPEP 2106 II-C*} storing either the partition information or user data depending on a configuration of the memory card;" **[Suda discloses this concept as "Fig. 1 shows the conventional memory card, in which flags are added to conventional reserved areas" (Page 3, paragraph 0039, lines 1-2) wherein "information indicating the corresponding storage area number is added hereto" (Page 3, paragraph 0039, lines 12-13) and "information indicating the quantity of**

the storage areas is added hereto"(Page 3, paragraph 0039, lines 25-26)]. Furthermore, Suda discloses Applicant should note that as the "internal register 18" stores the number of areas inside a memory card, this number of areas corresponds to the claimed "volume information." The number of areas inside a memory card represents the number of volumes inside a memory card, and therefore, represents "volume information." Furthermore, Suda discloses [***"FIG. 1 shows the conventional memory card, in which flags are added to convention reserved areas. Each of the internal registers 12a, 12b, 12c, and 12d of the memory card 3 includes first to third bit string 20a, 20b, and 20c... The first bit string 20a equivalent to the first 23 bits of the internal register indicates a characteristic of the memory card... The second bit string 20b equivalent to the first 23 bits of the internal register indicates a characteristic of the memory card 3… The third bit string 20c equivalent to 4 bits subsequent to the second bit string is also a convention reserved area of the internal register... Information indicating the quantity of storage areas is added hereto... In the memory card 3, shown in FIG. 1, a flag indicating 4 is et to each of the third bit strings of the internal register... when the memory card 3 has four storage areas"*** **(Par. 0039; See Figure 1 and related text)**]. Applicant should note that Examiner interprets the "first storage areas 11a-12a, 11b-12b, 11c-12c and 11d-12d" as a continuous address space which is shown as bit strings comprising fields 20a, 20b and 20c. Therefore, as Suda stores volume information indicating the number of storage areas within field 20c of internal registers, which are shown to comprise a contiguous range of addresses. Suda discloses [**"FIG. 5 shows the memory card 3 in which the plural storage areas 11a, 11b, and 11c severally include the internal registers 12a, 12b, and 12c" (Figure 5 and related text) wherein contiguous address space comprising addresses 00000-xFFFF is shown to**

include/encompass both storage areas 11a, 11b, 11c and internal registers 12a, 12b, and 12c, as shown in the citation above (Note that the drawing in Figure 5, included dashed lines does not exclude internal registers from address space shown on the left)]. Further, any memory/storage device is "capable of" storing any type of data. Furthermore, claims 1, 13 and 19 require that the contiguous range of the address space store either user data OR system configuration data, which is taught by Suda **[See above]**.

"a switch being set in one of a plurality of switch positions;" **[With respect to this limitation, Suda discloses "a large-capacity memory card which is arranged to switch plural storage areas with the use of mechanical switches provided on a housing" (Page 5, paragraph 0068, lines 2-3)]**

"and a controller that manages access to the data stored in said non-volatile data storage," **[Suda discloses this limitation as "the controller 10 receives a command and data from the memory card host device 1 through the bus 2, and controls the storage areas based on the command and the data to the memory card" (Page 2, paragraph 0028, lines 6-9)]**

"wherein said controller examines the partition information stored in said first partition to determine whether the memory card has a first configuration using the single partition in accordance with a first file format or a second configuration using the multiple partitions in accordance with a second file format based on the partition information," **[With respect to this limitation, Suda discloses having "information indicating the quantity of storage areas" (Page 3, paragraph 0039, lines 25-26) and explains that "the memory card host device 1 refers to the reserved areas in accordance with the response from the controller 10 and interprets the flags" (Page 3, paragraph 0040, lines 10-13) which indicate the amount of**

storage areas being used. "it is possible to maintain compatibility with a conventional memory card host device by setting the storage area having the file system that can be controlled by the conventional memory card host device as the storage area accessible when the power supply is turned on. Regarding the other storage areas, it is possible to moderate limitations of the storage capacities by changing the file systems thereof into file systems adopting new methods" (Page 5, paragraph 0066). Suda also explains that the size of storage areas "does not exceed the marginal capacity which can be handled by using a single file system. For example, when the FAT 16 is used as the file system, the marginal capacity is equal to 2 gigabytes" (Page 2, paragraph 0028, lines 14-17) and that "a conventional command length can only express an address up to the second storage area 11b. However, with the use of the address expressed with blocks enables expression of a large-capacity address" (Figure 5 and Page 4, paragraph 0057, lines 17-20); therefore, multiple volume address space has a first file format and single volume address space having a second file format] "wherein when said controller determines that the memory card has the first configuration, the address space of said non-volatile data storage is divided into multiple partitions, each of the plurality of partitions containing the partition information store in a respective rage of addresses therein, one of the multiple partitions being accessed based on the switch position of said switch," **[Suda discloses this limitation as when judgment determines that a plurality of storage areas exist, then "the memory card switches storage areas so as to refer to a desired storage area" (Page 3, paragraph 0034, lines 1-3) and explains that "when the area has changed normally," then "data processing of the memory card by the memory card host device is performed" (Page 3, paragraph 0035, lines 8-10). Suda also**

discloses "mechanical switches 16a and 16b for selecting one of the plural storage areas, and a controller 10 for reflecting the storage area selected by the mechanical switches" (Page 5, paragraph 0069, lines 1-4); thereby, operating the memory card as having a plurality of volumes wherein storage registers in each volume store volume information for each volume (See Above)].

wherein when said controller determines that the memory card has the second configuration using the single partition, the first partition being the single partition,

[With respect to this limitation, Suda discloses "where a judgment is made that there is only a single storage area, then normal processing takes place" (Pages 2-3, paragraph 0033, lines 10-11) and explains "in a memory card host device which cannot perform the above-described processing, the memory card remains in the state as shown in Fig. 4A when the power supply is turned on. Accordingly, such a memory card host device handles the memory card as the memory card having only the first storage area 11a" (Page 4, Par. 0050); thereby, operating the memory card as having a single volume. Note that any memory or storage area may be "used for storing any data type"]

Assuming (*for the sake of argument*) that Suda's internal registers were not included in the address space defined by the contiguous range of addresses 00000 through xFFFF, as argued by Applicant, it would be obvious to one of ordinary skill in the art to place internal registers within this range or anywhere within memory card 3, since it involves a simple relocation of parts and it has been held that rearranging parts of an invention involves only routine skill in the art. *In re Japikse,* 86 USPQ 70.

Suda does not disclose expressly wherein when said controller determines that the memory card has the second configuration using the single partition, the entire address space of said non-volatile data storage is accessed as a single partition, the first partition being the single partition, nor wherein each range of addresses which stores the partition information in a second and any subsequent partitions under the first configuration stores user data under the second configuration.

Moro discloses wherein when said controller determines that the memory card has the second configuration using the single partition, the entire address space of said non-volatile data storage is accessed as a single partition, the first partition being the single partition as **["the capacity switching-type memory card host device 12 performs a setting to make the first partition 162 and the second partition 163 accessible as a single partition... Concrete examples of the method for setting of the single partition are shown in FIG. 6... logically connecting three partitions of C: 801, D: 802, and E:803 and thereby qualifying these partitions collectively as a single partition C': 804" (par. 0038; figs. 1 and 6 and related text)]**.

Murray discloses **[merging two or more adjacent partitions to create a single or target partition wherein one or more FAT 16 partitions may be merged into a FAT 32 partition (col. 4, lines 37-55) and explains "a FAT files system normally places file system data 402 at or near the left edge of the partition; user data and available space (if any) take up the rest of the partition 400. The FAST file system data 402 in a target partition is modified when two or more FAT partitions are merged" (col. 7, lines 13-20) wherein "If the merged partition is to be a FAT partition, then the left-most partition is preferably**

considered the target partition because the merged FAT partition always places the combined system data on the left-hand side (near the start of the merged partition)" (col. 13, lines 18-46) "the target partition can be grown by moving its right edge (end)" (col. 10, lines 34-53). Also see (col. 15, line 57-col. 16, line 4; col. 17, line 63-col. 18, line 11; col. 18, lines 38-47). Murray also explain that data previously holding system data in a secondary partition is deleted to create free space for files/user data in the target partition (col. 20, line 23-col. 21, line 3). Also refer to (col. 22, line 45-col. 24, line 58)].

Suda, and Moro and Murray are analogous art because they are from the same field of endeavor of memory access and control.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify the memory card which can be accessed in either multiple mode or single mode, as described by Suda, and more specifically combine the multiple memory areas as a single memory area when using the memory card as a single volume, as taught by Moro, and further wherein each range of addresses which stores the partition information in a second and any subsequent partitions under the first configuration stores user data under the second configuration as taught by Murray.

The motivation for doing so would have been because Moro discloses providing the a memory card that can be used as multiple partitions or as a single partition provides the advantage of **[being able to increase the capacity of a memory and facilitate user access (pars. 0007 and 0038)]** and Murray discloses under a FAT files system, system information must be stored at the beginning of the volumes; thus, when combining two partitions into a target partition, system data must be moved to the beginning of the target partition and the rest is of the

area is freed to store files/user data as needed **[(col. 13, lines 18-46; col. 4, lines 37-55; col. 7, lines 13-20; col. 10, lines 34-53; col. 15, line 57-col. 16, line 4; col. 17, line 63-col. 18, line 11; col. 18, lines 38-47; col. 22, line 45-col. 24, line 58)]**.

Therefore, it would have been obvious to combine Suda with Moro and Murray for the benefit of creating a method for reading data from a memory card to obtain the invention as specified in claims 13-14, and 24.

16. As per **claim 18, and 25**, the combination of Suda, Moro and Murray discloses "A memory card as recited in claim 13," **[See rejection to claim 13 above]** "wherein said memory card is a FLASH memory device" **[With respect to this limitation, Suda discloses that "the memory card 3 corresponds to a secure digital (SD) memory card" (Page 2, paragraph 0029, lines 1-2) wherein "a copyright protection function corresponding to the secure digital music initiative (SDMI) standard, and is upward compatible with a multimedia card (MMC). The SD memory card is a memory card based on the SDMI standard which has been jointly developed by three companies Toshiba Corporation, Matsushita Electric Industrial Co., Ltd., and SanDisk Corporation" (Page 2, paragraph 0029) and explains addressing the memory card in block units instead of byte units (Page 4, paragraph 0057), which is equivalent to having a flash memory card]**.

17. As per **claims 19-20 and 22-24**, the rationale in the rejection to claims 1 and 13 is herein incorporated.

18. As per claims 36, 37 and 38, the combination of Suda, Moro and Murray discloses A method/memory card/memory device as recited in claims 1, 13 and 19 wherein said (c) operating the memory card in accordance with the first file format includes: mapping first volume

information onto a first address region of the address space; mapping second volume information onto a second address region of the address space, the second address region following the first address region;mapping first user data region for the first volume onto a third address region of the address space, the third address region following to the second address region; and mapping second user data region for the second volume onto a forth address region of the address space, the forth address region following to the third address region, and **[Suda discloses "*FIG. 1 shows the conventional memory card, in which flags are added to convention reserved areas. Each of the internal registers 12a, 12b, 12c, and 12d of the memory card 3 includes first to third bit string 20a, 20b, and 20c... The first bit string 20a equivalent to the first 23 bits of the internal register indicates a characteristic of the memory card... The second bit string 20b equivalent to the first 23 bits of the internal register indicates a characteristic of the memory card 3… The third bit string 20c equivalent to 4 bits subsequent to the second bit string is also a convention reserved area of the internal register... Information indicating the quantity of storage areas is added hereto... In the memory card 3, shown in FIG. 1, a flag indicating 4 is et to each of the third bit strings of the internal register... when the memory card 3 has four storage areas*" (Par. 0039; See Figure 1 and related text). Murray further discloses having multiple partitions wherein in a FAT system, system data at the start of the partition and user data in the rest of the memory space (col. 4, lines 37-55; col. 7, lines 13-20; col. 13, lines 18-46; col. 20, line 23-col. 21, line 3; Also refer to (col. 22, line 45-col. 24, line 58); see figs. 4-5 and related text]**

wherein said (d) operating the memory card in accordance with the second file format includes: mapping volume information for the single volume onto a fifth address region of the address

space, the fifth address region preceding the first address region; and mapping user data region for the single volume onto the second, third, and forth address regions of the address space **[Murray discloses merging two or more adjacent partitions to create a single or target partition wherein one or more FAT 16 partitions may be merged into a FAT 32 partition (col. 4, lines 37-55) and explains "a FAT files system normally places file system data 402 at or near the left edge of the partition; user data and available space (if any) take up the rest of the partition 400. The FAT file system data 402 in a target partition is modified when two or more FAT partitions are merged" (col. 7, lines 13-20) wherein "If the merged partition is to be a FAT partition, then the left-most partition is preferably considered the target partition because the merged FAT partition always places the combined system data on the left-hand side (near the start of the merged partition)" (col. 13, lines 18-46) "the target partition can be grown by moving its right edge (end)" (col. 10, lines 34-53). Also see (col. 15, line 57-col. 16, line 4; col. 17, line 63-col. 18, line 11; col. 18, lines 38-47). Murray also explain that data previously holding system data in a secondary partition is deleted to create free space for files/user data in the target partition (col. 20, line 23-col. 21, line 3). Also refer to (col. 22, line 45-col. 24, line 58)]**.

19. **Claims 11-12 and 15-16** are rejected under 35 U.S.C. 103(a) as being unpatentable over Suda (US 2004/0123059) in view of Moro (US 2004/0107316) and Murray et al. (US 6,185,666), and further in view of Colligan et al. (US 6,519,762).

20. As per **claims 11-12, and 15-16**, the combination of Suda, Moro and Murray discloses "A method as recited in claim 1, 13 and 30-31," **[See rejection to claim 1 above]** wherein when said determining (b) determines that the single volume address space is present on the memory

card, the first volume has a FAT-32 file format" and "wherein when said determining (b) determines that the multiple volume address space is present on the memory card, each of the multiple volumes having a FAT-16 file format" **[Suda teaches this limitation as "when a memory card host device applies a certain file system and the maximum capacity which the file system can handle is .alpha., then the first embodiment enables the memory card host device to handle a memory card having a total capacity larger than .alpha. by having a configuration with plural storage areas each having a capacity less than .alpha. inside the memory card enabling the handling of a total capacity larger than .alpha.." (Page 2, paragraph 0025) as teaching a memory that can adopt any type of file system present in a host device connected to the memory card. Suda also provides an example in which "FAT 16 is used as the file system" (Page 2, paragraph 0028). Moro discloses first partition using FAT 16, second partition using FAT 32 and combining these into a single partition (see figs. 1 and 6 and related text)]**. Murray discloses merging one ore more FAT 16 partitions into a FAT 32 partition **[(col. 4, lines 44-55)]**.

To further detail the combination of Suda, Moro and Murray, Colligan discloses wherein when said determining (b) determines that the single volume address space is present on the memory card, the first volume has a FAT-32 file format" and "wherein when said determining (b) determines that the multiple volume address space is present on the memory card, each of the multiple volumes having a FAT-16 file format" as **[a memory device including a single partition using FAT 32 or multiple partitions using FAT 16 (See figs. 2-3 and related text; col. 8, lines 5-13)]**.

Suda, Moro, Murray and Colligan are analogous art in that they are of the same field of endeavor, that is, a system and/or method of memory control. Colligan suggests that it would have been desirable to incorporate the ability of providing a single partition as FAT 32 or multiple partitions as FAT16 into the combined system of Suda, Moro and Murray because this would enable efficient partitioning of the system into different sized areas according to the file system used (col. 8, lines 11-14). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the combination of Suda and Moro as suggested by Colligan to incorporate the feature as claimed.

ACKNOWLEDGMENT OF ISSUES RAISED BY THE APPLICANT

Response to Amendment

21. Applicant's arguments filed on October 2, 2008 with respect to claims **1-25 and 36-38** have been fully considered but they are moot in view of new grounds of rejection.

22. As required by **M.P.E.P. § 707.07(f)**, a response to these arguments appears below.

ARGUMENTS CONCERNING PRIOR ART REJECTIONS

23. Claims must be given the broadest reasonable interpretation during examination and limitations appearing in the specification but not recited in the claim are not read into the claim (See M.P.E.P. 2111 [R-1]).

NOTE

24. The phrases "is configured to" "being capable of" and "used to" are interpreted as intended use, and as such the claims do not require that the system actually perform the listed functionality, but merely that the functionality not be expressly precluded. See MPEP 2106 II(C).

25. All arguments by the applicant are believed to be covered in the body of the office action; thus, this action constitutes a complete response to the issues raised in the remarks dated October 2, 2008.

CLOSING COMMENTS

Examiner's Note

26. Examiner has cited particular columns and line numbers in the references as applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings in the art and are applied to the specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant, in preparing the responses, to fully consider the references in entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the examiner.

Conclusion

a. STATUS OF CLAIMS IN THE APPLICATION

27. The following is a summary of the treatment and status of all claims in the application as recommended by **M.P.E.P. 707.07(i)**:

a(1) CLAIMS REJECTED IN THE APPLICATION

28. Per the instant office action, claims 1-25 and 36-38 have received a first action on the merits and are subject of a non-final rejection.

a(2) CLAIMS NO LONGER UNDER CONSIDERATION

29. Claims 26-35 stand canceled as of the amendment dated October 2, 2008.

b. DIRECTION OF FUTURE CORRESPONDENCES

30. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yaima Campos whose telephone number is (571) 272-1232. The examiner can normally be reached on Monday to Friday 8:30 AM to 5:00 PM.

IMPORTANT NOTE

31. If attempts to reach the above noted Examiner by telephone are unsuccessful, the Examiner's supervisor, Mr. Sanjiv Shah, can be reached at the following telephone number: Area Code (571) 272-4098.

The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

December 8, 2008

/Yaima Campos/
Examiner, Art Unit 2185

/Sanjiv Shah/

Supervisory Patent Examiner, Art Unit 2185